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Trigger Electronics for MIPP Upgrade

This document describes preliminary considerations for the design of the trigger electronics modules for the proposed MIPP upgrade (P-960). The current MIPP trigger system uses the following sources of the detector signals to generate a trigger:

- 12 Time-Of-Flight scintillation counters with PMTs
- 20 Veto scintillation counters with PMTs
- 4 Beam Cherenkov counters with PMTs

The PMT signals will be discriminated by commercial electronics modules available from Fermilab PREP. The logic combinations of the discriminators outputs will be used to generate trigger output signals using MIPP Logic module. The MIPP Logic module will provide the following functionality:

- Double width 6U VME module
- 32 NIM/TTL programmable logic inputs with LEMO connectors
- 4 NIM programmable logic outputs with LEMO connectors
- 8 channels of 0.5 ns time measurements for selected input channels
- Internal memory storage for default power-up configuration

The module has a VME slave interface and implemented as a double width 6U VME board. The outputs of the MIPP Logic modules will be fed to the MIPP Trigger module. This module will be responsible for the generation and distribution of the trigger signals to the MIPP Readout Controller modules. The MIPP Trigger module will provide the following functionality:

- Double width 6U VME module
- 16 trigger logic NIM/TTL signal inputs with LEMO connectors
- Two Beam synchronization signals (RF, TCLK) with LEMO connectors
- TCLK events decoder
- One RJ-45 input connector

- 8 RJ-45 output connectors
- Programmable trigger pre-scalers
- Various input/output signal scalers
- Internal FIFO memory for the trigger condition of the individual triggers
- Internal memory storage for default power-up configuration

The MIPP Trigger module receives and encodes 16-NIM/TTL input signals as experiment triggers. The definition of various triggers is provided in reference [1]. In addition to the trigger signal, the module generates a sequence of timing control signals also encoded into the RF/2 clock signal [2]. The main signals are Begin-Of-Spill (BOS) and End-Of-Spill (EOS). The BOS and EOS indicate the beginning and the end of the active beam cycle respectively. The encoded trigger signals should be generated only between BOS and EOS signals.

Asynchronous to the beam INIT, Global Reset and Read Event logic level signals are distributed directly via RJ-45 connector. These signals are to be received and encoded by the Readout Controller Module, and distributed to the front-ends along with the other clock-embedded control signals. The Readout Controller Module may generate Global Reset and Read Event signals independently. The Trigger Module has an internal quartz oscillator, which could be either locked to the accelerator RF or set to a free running mode. The timing sequencer generating beam related signals could be synchronized to the BSCLK events (e.g. $75) or set to run free with a programmable repetition rate.

The MIPP Trigger Module has one RJ-45 input and eight RJ-45 output modular connectors. It can be used as a fanout module do distribute timing and control signals within MIPP DAQ crates. The module has a VME slave interface and implemented as a double width 6U VME board. The four signals on RJ-45 connectors have LVDS levels and are listed in the Table 1.

Table 1 RJ-45 connector pinouts

No.	Signal Name	Pin	Comment
1	RFTM+	1	Encoded RF, LVDS
2	RFTM-	2	Encoded RF, LVDS
3	GRST+	4	Global Reset, LVDS
4	GRST-	5	Global Reset, LVDS

5	RDEV+	3	Read Event, LVDS
6	RDEV-	6	Read Event, LVDS
7	INIT +	7	Initialize, LVDS
8	INIT -	8	Initialize, LVDS

References

[1] Holger Meyer, “Specifications for MIPP readout electronics back end communication,” MIPP-doc-186, April 2007, MIPP document database

[2] B.Baldin, S.Hansen, “MIPP Data Cable Protocol,” MIPP-doc-764, April 2008, MIPP document database